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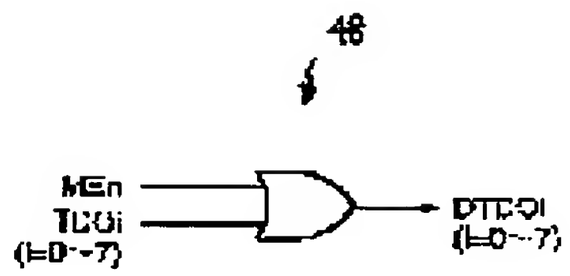
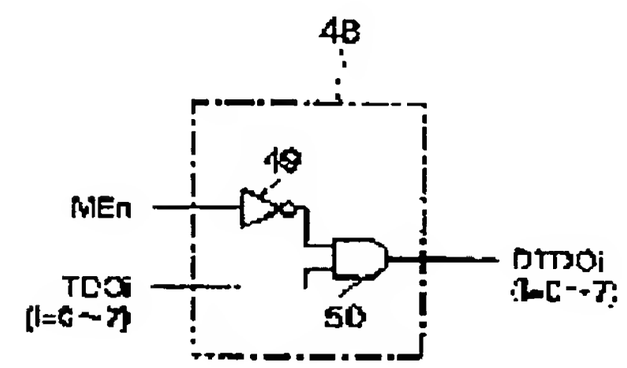
(54) MEMORY HYBRID LOGIC LSI

(57)Abstract:
PROBLEM TO BE SOLVED: To shorten a test time and simplify a test by generating a plurality of memory macros and a macro ID for identifying the plurality of memory macros in one chip outside the plurality of memory macros, and electrically connecting one of the plurality of memory macros to an output pad.
SOLUTION: At a selected memory macro, MEn=0 is input to a macro output control circuit 48 and an 8-bit output signal which is a direct selection of TDO(0-7) is output as an output signal DTDO(0-7) of the memory macro. At a non selected memory macro, MEn=1 is input to the macro output control circuit 48, and therefore the output signal DTDO(0-7) of the non selected memory macro is fixed to '1' irrespective of the 8-bit output signal TDO(0-7). The signal of '1' or '0' is fed to a logic part from the selected memory macro, and the output signal of '1' is fed from the non selected memory macro.





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